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Hirakayashi et al

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TITLE: Positive stagger type **thin film transistor** manufacturing method, involves **removing** protrusion of **polysilicon** film by chemo mechanical polishing

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PRIORITY-DATA: 1998JP-0209607 (July 24, 1998)

PATENT-FAMILY:

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INT-CL (IPC): H01L021/304, H01L021/336 , H01L029/786

ABSTRACTED-PUB-NO: JP2000040828A

BASIC-ABSTRACT:

NOVELTY - **Polysilicon** thin film with a protrusion on its surface is formed by irradiating **amorphous silicon** thin film on glass substrate (11). The protrusion on the surface is **removed** by chemo mechanical polishing by using polish slurry, which contains polish **grinding** particles for polarization of the surface of the **polysilicon** thin film.

DETAILED DESCRIPTION - The polish liquid slurry containing polish grinding particles consisting of silica, is adjusted by pHs 10-11.

USE - for manufacturing positive stagger type **thin film transistor** used in liquid crystal display device.

ADVANTAGE - Since the **polysilicon** thin film surface of mobility of carrier is polarized, the gate insulating film with favorable isolated breakdown voltage, is formed on the activated layer, thereby providing reliable positive stagger type **thin film transistor**.

DESCRIPTION OF DRAWING - The figure shows sectional view of manufacturing method of positive stagger type **thin film transistor**. (11) Glass substrate.

CHOSEN-DRAWING: Dwg.3/3

TITLE-TERMS: POSITIVE STAGGER TYPE **THIN FILM TRANSISTOR** MANUFACTURE METHOD REMOVE PROTRUDE FILM CHEMICO MECHANICAL POLISH

DERWENT-CLASS: L03 U11 U12

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EPI-CODES: U11-C06A1A; U11-C18A3; U12-B03A;

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TITLE: PRODUCTION METHOD OF THIN FILM TRANSISTOR

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ABSTRACT:

PROBLEM TO BE SOLVED: To provide a production method of a positive stagger-type thin film transistor which can form a gate insulating film having good dielectric strength on an active layer composed of a polysilicon thin film by leveling the surface of the polysilicon thin film featuring high mobility of a carrier.

SOLUTION: The production method of a thin film transistor consists of the following processes: a process wherein an amorphous silicon thin film acting as an insulating film is formed on a glass substrate 11; a process wherein a polysilicon thin film 13 having projections 14 is formed on the surface of the amorphous silicon thin film by poly-crystallization through irradiation of the amorphous thin film with energy beams; and a process wherein the surface of the polysilicon thin film 13 is leveled by removal of the projections 14 on the surface of the polysilicon thin film 13 by chemical mechanical polishing with the use of an abrasive slurry containing abrasive grains.

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21/336		21/304	６２２Ｘ	
21/304	６２２	29/78	６２７Ａ	

審査請求　未請求　請求項の数３　ＯＬ　（全５頁）

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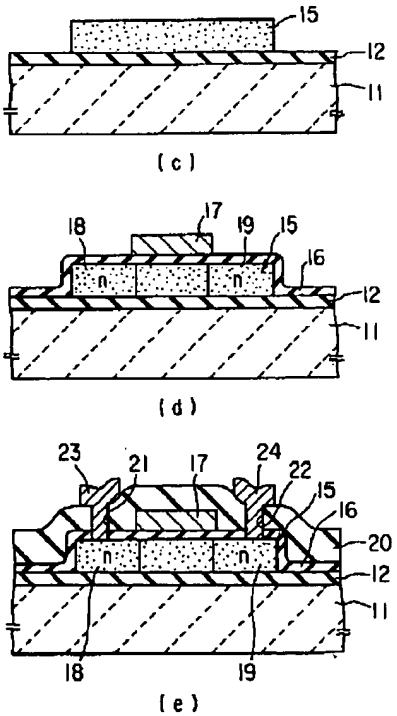
(54)【発明の名称】　薄膜トランジスタの製造方法

(57)【要約】
【課題】　キャリアのモビリティの高いポリシリコン薄膜表面を平坦化することにより、このポリシリコン薄膜からなる活性層上に良好な絶縁耐圧を有するゲート絶縁膜を形成することが可能な正スタガ型の薄膜トランジスタの製造方法を提供しようとものである。
【解決手段】　ガラス基板上の絶縁膜にアモルファスシリコン薄膜を成膜する工程と、前記アモルファスシリコン薄膜にエネルギービームを照射して多結晶化して表面に突起を有するポリシリコン薄膜を形成する工程と、前記ポリシリコン薄膜表面の突起を研磨砥粒を含む研磨スラリーを用いた化学機械研磨により除去して前記ポリシリコン薄膜表面を平坦化する工程とを具備したことを特徴とするものである。



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【特許請求の範囲】

【請求項１】　ガラス基板上の絶縁膜にアモルファスシリコン薄膜を成膜する工程と、

前記アモルファスシリコン薄膜にエネルギービームを照射して多結晶化してポリシリコン薄膜を形成する工程と、

前記ポリシリコン薄膜表面の突起を研磨砥粒を含む研磨スラリーを用いた化学機械研磨により除去して前記ポリシリコン薄膜表面を平坦化する工程とを具備したことを特徴とする薄膜トランジスタの製造方法。

【請求項２】　前記研磨液スラリーは、シリカからなる研磨砥粒を含むｐＨ１０～１１に調節されたものであることを特徴とする請求項１記載の薄膜トランジスタの製造方法。

【請求項３】　前記化学機械研磨は、２０～１０００ｋｇ／ｃｍ^2 の圧力でなされることを特徴とする請求項２記載の薄膜トランジスタの製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、液晶表示装置に組込まれる薄膜トランジスタの製造方法に関し、特に活性層を改良した正スタガ型の薄膜トランジスタの製造方法に係わる。

【０００２】

【従来の技術】液晶表示装置に組込まれる正スタガ型薄膜トランジスタは、従来よりソース、ドレイン領域が形成される活性層をアモルファスシリコン（以下、ａ－Ｓｉと称す）薄膜により形成していた。しかしながら、ａ－Ｓｉ薄膜はトランジスタ特性に大きな影響を与えるキャリアの移動度が小さいという問題があった。

【０００３】このようなことから、近年、液晶表示装置の薄膜トランジスタの特性（キャリアのモビリティ）を向上させるために活性層をポリシリコン薄膜で形成する技術の開発が進んでいる。このポリシリコン薄膜の形成技術としては、ガラス基板上の絶縁膜にａ－Ｓｉ薄膜を成膜した後、レーザビームのようなエネルギービームを照射することにより多結晶化する方法が知られている。

【０００４】しかしながら、前記方法により得られたポリシリコン薄膜は表面に数十ｎｍの突起が発生する。このため、このポリシリコン薄膜をパターニングして活性層を形成し、その上にゲート絶縁膜、ゲート電極を形成した後、前記活性層にソース、ドレイン領域を形成して正スタガ型の薄膜トランジスタを製造すると、前記ポリシリコンからなる活性層表面の突起に起因して前記ゲート絶縁膜の耐圧不良を生じ、トランジスタ特性が著しく低下する。

【０００５】

【発明が解決しようとする課題】本発明の目的は、キャリアのモビリティの高いポリシリコン薄膜表面を平坦化することにより、このポリシリコン薄膜からなる活性層上に良好な絶縁耐圧を有するゲート絶縁膜を形成することが可能な正スタガ型の薄膜トランジスタの製造方法を提供しようとするものである。

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【０００６】

【課題を解決するための手段】本発明に係わる薄膜トランジスタの製造方法は、ガラス基板上の絶縁膜にアモルファスシリコン薄膜を成膜する工程と、前記アモルファスシリコン薄膜にエネルギービームを照射して多結晶化してポリシリコン薄膜を形成する工程と、前記ポリシリコン薄膜表面の突起を研磨砥粒を含む研磨スラリーを用いた化学機械研磨により除去して前記ポリシリコン薄膜表面を平坦化する工程とを具備したことを特徴とするものである。

【０００７】

【発明の実施の形態】以下、本発明に係わる薄膜トランジスタの製造方法を詳細に説明する。

（第１工程）まず、ガラス基板上の酸化ケイ素のような絶縁膜にａ－Ｓｉ薄膜をＣＶＤ法等により成膜する。

【０００８】前記ガラス基板上には、前記絶縁膜の被覆前に予めゲート電極を形成することを許容する。

（第２工程）次いで、前記ａ－Ｓｉ薄膜にエネルギービームを照射する。この時、前記ａ－Ｓｉ薄膜は、多結晶化して結晶性が良好なポリシリコン薄膜に変換される。同時に表面に数十ｎｍオーダの突起が発生する。

【０００９】前記エネルギービームとしては、例えばレーザビーム、電子ビーム等を用いることができる。

（第３工程）次いで、前記ポリシリコン薄膜表面を研磨砥粒を含む研磨スラリーを用いた化学機械研磨（ＣＭＰ；Chemical Mechanical Polishing）することにより前記突起を除去して前記ポリシリンコ薄膜の表面を平坦化する。

【００１０】前記ＣＭＰに適用されるポリシング装置としては、例えば図１に示す構造のものが用いられる。このポリシング装置は、ターンテーブル１を有する。このターンテーブル１上には、例えば布から作られた研磨パッド２が被覆されている。研磨液を供給するための供給管３は、前記研磨パッド２の上方に配置されている。上面に支持軸４を有する基板ホルダ５は、研磨パッド２の上方に上下動自在でかつ回転自在に配置されている。

【００１１】このようなポリシング装置において、前記ホルダ５により基板６をその研磨面であるポリシリコン薄膜が前記研磨パッド２に対向するように保持し、前記供給管３から前述した組成の研摩液７を供給しながら、前記支持軸４により前記基板６を前記研磨パッド２に向けて所望の加重を与え、さらに前記ホルド５および前記ターンテーブル１を互いに反対方向に回転させることにより前記基板６上のポリシリコン薄膜表面の突起が除去される。

【００１２】前記研磨砥粒としては、シリカ、ジルコニア、酸化セリウムおよびアルミナから選ばれる少なくと

も1つの材料の粒子を用いることができる。これらの粒子は、0．02～0．1μmの平均粒径を有し、球状もしくは球に近似した形状を有することが好ましい。

【0013】前記研磨砥粒は、前記研磨スラリー中に0．1～30重量%含有されることが好ましい。前記研磨砥粒の含有量を0．1重量%未満にすると、その効果を十分に達成することが困難になる。一方、前記研磨砥粒の含有量が30重量%を越えると、研磨液の粘度等が高くなって取扱い難くなる。より好ましい前記研磨砥粒の含有量は、1～10重量%である。

【0014】前記研磨砥粒は、特にシリカ粒子（好ましくは平均粒径0．01～0．09μmのコロイダルシリカ）が望ましい。このようなシリカ粒子からなる研磨砥粒を用いた場合には、前記研磨スラリーのpHを10～11にすることが好ましい。

【0015】前記CMPにおける圧力（前述した図1におけるポリシリコン薄膜の研磨パッド2への加重）は、20～1000kg／cm^2 にすることが好ましい。前記圧力を20kg／cm^2 未満にすると、前記ポリシリコン薄膜の突起を除去することが困難になる。一方、前記圧力が1000kg／cm^2 を超えると、ポリシリコン薄膜にクラックが発生したり、ポリシリコン薄膜の厚さが減少する、いわゆる膜減りを生じる恐れがある。より好ましい前記圧力は、50～200kg／cm^2 である。

【0016】（第4工程）前述した表面が平坦なポリシリコン薄膜をフォトエッチングプロセスによりパターニングして活性層を形成した後、前記活性層の少なくとも上面にゲート絶縁膜を形成する。つづいて、前記活性層に対応するゲート絶縁膜上にゲート電極を形成した後、例えば前記ゲート電極をマスクとして前記活性層に導電性を与える不純物をイオン注入してソース、ドレイン領域を形成する。ひきつづき、全面に例えばCVD法により層間絶縁膜を堆積する。その後、前記ソース、ドレイン領域に対応する前記層間絶縁膜部分にコンタクトホールを開口し、電極用金属の被覆、パターニングにより前記ソース、ドレイン領域に前記コンタクトホールを通して接続されるソース、ドレイン電極を形成することにより正スタガ型の薄膜トランジスタを製造する。

【0017】以上説明した本発明によれば、ガラス基板上の絶縁膜にアモルファスシリコン薄膜を成膜し、このアモルファスシリコン薄膜にエネルギービームを照射して多結晶化して表面に突起を有するポリシリコン薄膜を形成し、このポリシリコン薄膜表面の突起を研磨砥粒を含む研磨スラリーを用いた化学機械研磨により除去することによって、表面が平坦化されたポリシリコン薄膜にすることができる。このようなポリシリコン薄膜をパターニングして活性層を形成し、その上にゲート絶縁膜、ゲート電極を形成した後、前記活性層にソース、ドレイン領域を形成することによって、前記ポリシリコン薄膜

表面の突起に起因する前記ゲート絶縁膜の絶縁耐圧不良を抑制ないし解消した良好な特性を有する正スタガ型の薄膜トランジスタを製造することができる。

【0018】特に、前記ポリシリコン薄膜のCMP工程においてシリカ粒子を研磨砥粒として含有し、pHが10～11の研摩スラリーを用いることによって、前記シリカ粒子が前記ポリシリコン薄膜の突起と反応するため、機械的研磨により前記反応物がポリシリコン薄膜から剥離除去される。つまり、前記ポリシリコン薄膜の突起が選択的に除去されてポリシリコン薄膜自体の膜減りを防止することができる。

【0019】また、前記ポリシリコン薄膜のCMP工程において圧力（前述した図1におけるポリシリコン薄膜の研磨パッド2への加重）を20～1000kg／cm^2 にすることによって、前記ポリシリコン薄膜のクラック発生およびポリシリコン薄膜の膜減りを防止することが可能になる。

【0020】

【実施例】以下、本発明の好ましい実施例を図面を参照しして詳細に説明する。

（実施例1）まず、図2の（a）に示すようにガラス基板11上にCVD法によりSiO_2膜12を成膜した後、前記SiO_2 膜12にCVD法により厚さ0．05μmのアモルファスシリコン（a－Si）薄膜を成膜した。つづいて、このa－Si薄膜にエネルギー密度250～400mJ／cm^2 、パルス巾20～30nmのレーザビームを照射した。その結果、前記a－Si薄膜が多結晶化されてポリシリコン薄膜13に変換されるとともに、表面に突起14が発生された。

【0021】次いで、前述した図1に示すポリシング装置の基板ホルダ5に図2の（a）に示す基板11を逆さにして保持し、前記ホルダ5の支持軸4により前記基板をターンテーブル1上のローデル社製商品名；Suba 400からなる研磨パッド2に100g／cm^2 の加重を与え、前記ターンテーブル1およびホルダ5をそれぞれ60rpmの速度で互いに反対方向に回転させながら、コロイダルシリカを含む研磨スラリー（フジミ社製商品名；SP－15，pH＝11）を供給管3から20mL／分の速度で前記研磨パッド2に供給するCMP操作を20秒間行なって前記基板11のポリシリコン薄膜13の突起を除去することにより図2の（b）に示すようにポリシリコン薄膜13の表面を平坦化した。

【0022】前記CMP処理前後のポリシリコン薄膜における5箇所の表面粗さおよびP－V（最大凸部と最小凹部の間の高さ）を光学式表面粗さ計（Zygo）で調べた。また、それらの5点平均値を求めた。その結果を下記表1に示す。

【0023】

【表1】

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	研磨前		研磨後	
	表面粗さ（nm）	P－V（nm）	表面粗さ（nm）	P－V（nm）
No. 1	3.921	23.666	1.094	7.056
No. 2	2.503	18.744	1.107	7.087
No. 3	2.705	15.819	1.014	5.523
No. 4	2.364	15.299	1.099	6.383
No. 5	2.376	16.183	1.315	8.395
平均	2.774	17.942	1.126	6.885

【００２４】前記表１から明らかなように多結晶化後のポリシリコン薄膜の５点平均Ｐ－Ｖは１８ｎｍであったのに対し、研磨後においてはその５点平均Ｐ－Ｖが約７ｎｍになり、ポリシリコン薄膜表面が平坦化されることがわかる。

【００２５】次いで、図３の（ｃ）に示すように前記ポリシリコン薄膜１３をフォトエッチングプロセスによりパターニングして活性層１５を形成した。つづいて、前記活性層１５を含む全面にＣＶＤ法により厚さ０．１５μｍのSiO_2膜（ゲート絶縁膜）１６を形成した後、厚さ０．２５μｍのＭｏＷ膜を堆積し、パターニングすることによりゲート電極１７を形成した。ひきつづき、前記ゲート電極１７をマスクとして前記活性層１５にリンをイオン注入し、活性化することにより図３の（ｄ）に示すｎ型のソース、ドレイン領域１８，１９を形成した。

【００２６】次いで、全面に例えばＣＶＤ法によりSiO_2膜からなる層間絶縁膜２０を堆積した。その後、前記ソース、ドレイン領域１８，１９に対応する前記層間絶縁膜２０部分にコンタクトホール２１，２２を開口し、Ａｌ膜の堆積、パターニングを施すことにより前記ソース、ドレイン領域１８，１９に前記コンタクトホール２１，２２を通して接続されるソース、ドレイン電極２３，２４を形成することにより図３の（ｅ）に示す正スタガ型の薄膜トランジスタを製造した。

【００２７】（比較例１）活性層としてＣＭＰ処理を施さない表面に突起が発生したポリシリコン薄膜により形成した以外、実施例１と同様な方法により正スタガ型の薄膜トランジスタを製造した。

【００２８】得られた実施例１および比較例１の薄膜トランジスタのゲート絶縁膜の絶縁耐圧を測定したところ、実施例１の薄膜トランジスタは比較例１の薄膜トランジスタに比べてきわめて高い絶縁耐圧を示すことが確認された。

【００２９】

【発明の効果】以上説明したように、本発明によればキャリアのモビリティの高いポリシリコン薄膜表面を平坦化することにより、このポリシリコン薄膜からなる活性層上に良好な絶縁耐圧を有するゲート絶縁膜を形成することができ、ひいては信頼性の高い正スタガ型の薄膜トランジスタの製造方法を提供できる。

【図面の簡単な説明】

【図１】本発明のＣＭＰ工程に使用されるポリシング装置を示す概略図。

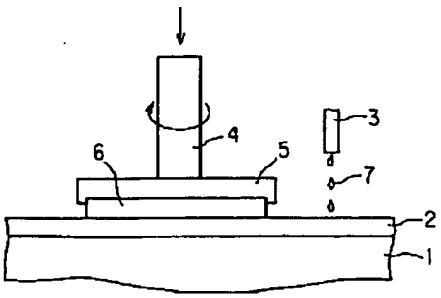
【図２】本発明の実施例１における正スタガ型薄膜トランジスタの製造工程を示す断面図。

【図３】本発明の実施例１における正スタガ型薄膜トランジスタの製造工程を示す断面図。

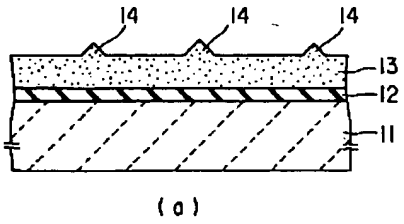
【符号の説明】

１…ターンテーブル、
２…研磨パッド、
３…供給管、
５…ホルダ、
１１…ガラス基板、
１３…ポリシリコン薄膜、
１４…突起、
１５…活性層、
１６…ゲート絶縁膜、
１７…ゲート電極。

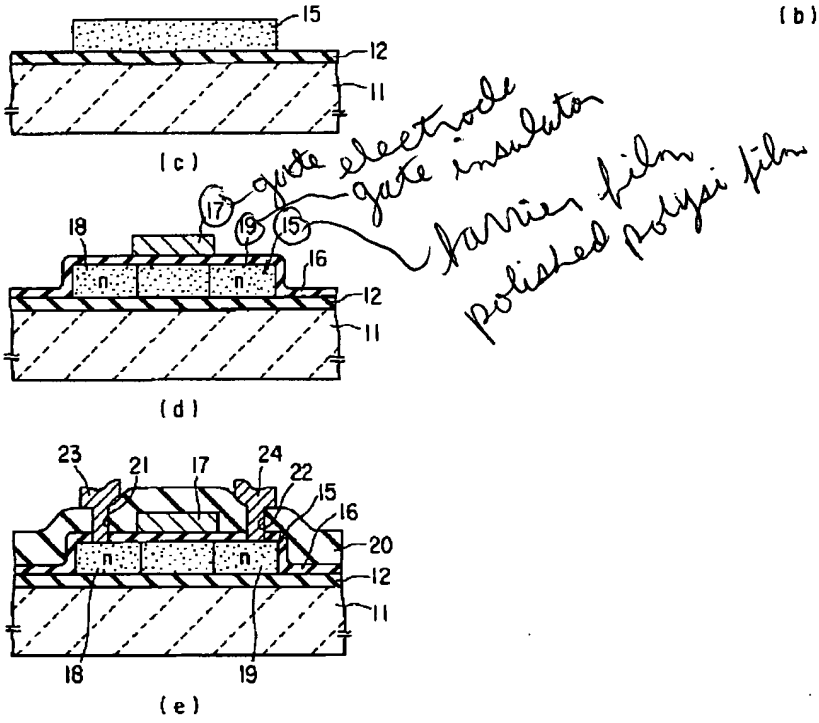
【図1】


3
4
5
6
7
2
1

【図2】


14
14
14
13
12
11
(a)
14
25
11
(b)

【図3】


15
12
11
(c)
17
19
15
18
16
n
n
12
11
(d)
23
21
17
24
22
15
16
20
n
n
12
11
18
19
(e)
gate electrode
gate insulator
barrier film
polished polysi film

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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the thin film transistor characterized by providing the process which forms an amorphous silicon thin film to the insulator layer on a glass substrate, the process which irradiates a energy beam, polycrystal-izes it to said amorphous silicon thin film, and forms a polish recon thin film, and the process which removes the projection of said polish recon thin film front face by chemical machinery polish using the polish slurry containing a polish abrasive grain, and carries out flattening of said polish recon thin film front face.
[Claim 2] Said polish liquid slurry is the manufacture approach of the thin film transistor according to claim 1 characterized by being adjusted by pH 10-11 containing the polish abrasive grain which consists of a silica.
[Claim 3] Said chemical machinery polish is 20-1000kg/cm2. The manufacture approach of the thin film transistor according to claim 2 characterized by being made by the pressure.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of the thin film transistor of a forward stagger mold of having improved especially the barrier layer, about the manufacture approach of the thin film transistor included in a liquid crystal display.
[0002]
[Description of the Prior Art] The forward stagger mold thin film transistor included in a liquid crystal display formed the barrier layer in which the source and a drain field are formed conventionally with the amorphous silicon (a-Si is called hereafter) thin film. However, the a-Si thin film had the problem that the mobility of the carrier which has big effect on transistor characteristics was small.
[0003] Since it is such, in order to raise the property (mobility of a carrier) of the thin film transistor of a liquid crystal display in recent years, development of the technique which forms a barrier layer with a polish recon thin film is progressing. As a formation technique of this polish recon thin film, after forming an a-Si thin film to the insulator layer on a glass substrate, the approach of polycrystal-izing is learned by irradiating a energy beam like a laser beam.
[0004] However, a dozens of nm projection generates the polish recon thin film obtained by said approach on a front face. For this reason, if the source and a drain field are formed in said barrier layer and the thin film transistor of a forward stagger mold is manufactured after carrying out patterning of this polish recon thin film, forming a barrier layer and forming gate dielectric film and a gate electrode on it, it will originate in the projection on the front face of a barrier layer which consists of said polish recon, the poor proof pressure of said gate dielectric film will be produced, and transistor characteristics will fall remarkably.
[0005]
[Problem(s) to be Solved by the Invention] The purpose of this invention tends to offer the manufacture approach of the thin film transistor of the forward stagger mold which can form the gate dielectric film which has good withstand voltage on the barrier layer which consists of this polish recon thin film by carrying out flattening of the high polish recon thin film front face of the mobility of a carrier.
[0006]
[Means for Solving the Problem] The manufacture approach of the thin film transistor concerning this invention is characterized by to provide the process which forms an amorphous silicon thin film to the insulator layer on a glass substrate, the process which irradiates a energy beam, polycrystal-izes it to said amorphous silicon thin film, and forms a polish recon thin film, and the process which removes the projection of said polish recon thin film front face by chemical-machinery polish using the polish slurry containing a polish abrasive grain, and carries out flattening of said polish recon thin film front face.
[0007]
[Embodiment of the Invention] Hereafter, the manufacture approach of the thin film transistor concerning this invention is explained to a detail.
(The 1st process) An a-Si thin film is first formed with a CVD method etc. to an insulator layer like the silicon oxide on a glass substrate.
[0008] It permits forming a gate electrode beforehand before covering of said insulator layer on said glass substrate.
(The 2nd process) Subsequently to said a-Si thin film, a energy beam is irradiated. At this time, said a-Si thin film is polycrystal-ized, and is changed into a polish recon thin film with good crystallinity. The projection of dozens of nm order occurs on a front face in coincidence.
[0009] As said energy beam, a laser beam, an electron beam, etc. can be used, for example.

(The 3rd process) By [which subsequently used the polish slurry which includes said polish recon thin film front face for a polish abrasive grain] carrying out chemical machinery polish (CMP;Chemical Mechanical Polishing), said projection is removed and flattening of the front face of said polish RINKO thin film is carried out.
[0010] As polishing equipment applied to said CMP, the thing of the structure shown, for example in drawing 1 is used. This polishing equipment has a turntable 1. On this turntable 1, the scouring pad 2 made from cloth is covered. The supply pipe 3 for supplying polish liquid is arranged above said scouring pad 2. The substrate holder 5 which has the support shaft 4 on the top face is arranged can move up and down freely above a scouring pad 2, and free [rotation].
[0011] Supplying the polishing liquid 7 of the presentation which held in such polishing equipment so that the polish recon thin film which is the polished surface might counter said scouring pad 2 in a substrate 6 with said holder 5, and was mentioned above from said supply pipe 3 Said substrate 6 is turned to said scouring pad 2 with said support shaft 4, a desired load is given, and the projection of the polish recon thin film front face on said substrate 6 is removed by making an opposite direction rotate said HORUDO 5 and said turntable 1 of each other further.
[0012] As said polish abrasive grain, the particle of at least one ingredient chosen from a silica, a zirconia, cerium oxide, and an alumina can be used. These particles have the mean particle diameter of 0.02-0.1 micrometers, and it is desirable spherical or to have the configuration approximated to the ball.
[0013] As for said polish abrasive grain, it is desirable to contain 0.1 to 30% of the weight in said polish slurry. If the content of said polish abrasive grain is carried out to less than 0.1% of the weight, it will become difficult to fully attain the effectiveness. On the other hand, if the content of said polish abrasive grain exceeds 30 % of the weight, the viscosity of polish liquid etc. will become high and it will be hard coming to deal with it. The content of said more desirable polish abrasive grain is 1 - 10 % of the weight.
[0014] Said especially polish abrasive grain has a desirable silica particle (preferably colloidal silica with a mean particle diameter of 0.01-0.09 micrometers). When the polish abrasive grain which consists of such a silica particle is used, it is desirable to set pH of said polish slurry to 10-11.
[0015] The pressure (load to the scouring pad 2 of the polish recon thin film in drawing 1 mentioned above) in said CMP is 20-1000kg/cm2. Carrying out is desirable. It is said pressure 20kg/cm2 If it is made the following, it will become difficult to remove the projection of said polish recon thin film. On the other hand, said pressure is 1000kg/cm2. When it exceeds, a crack occurs in a polish recon thin film, or a possibility that the thickness of a polish recon thin film decreases and of producing the so-called film decrease is in it. said more desirable pressure -- 50-200kg/cm2 it is .
[0016] (The 4th process) said barrier layer after the front face mentioned above carries out patterning of the flat polish recon thin film according to a photo etching process and forms a barrier layer -- gate dielectric film is formed in a top face at least. After continuing and forming a gate electrode on the gate dielectric film corresponding to said barrier layer, the ion implantation of the impurity which gives conductivity to said barrier layer by using said gate electrode as a mask is carried out, and the source and a drain field are formed. It pulls, and it continues and an interlayer insulation film is deposited on the whole surface with a CVD method. then, said interlayer insulation film part corresponding to said source and a drain field -- a contact hole -- opening -- carrying out -- an electrode -- public funds -- the thin film transistor of a forward stagger mold is manufactured by forming the source and the drain electrode which are connected to said source and a drain field through said contact hole by covering of a group, and patterning.
[0017] A front face can make it the polish recon thin film by which flattening was carried out by according to this invention explained above, forming an amorphous silicon thin film to the insulator layer on a glass substrate, forming the polish recon thin film which irradiates a energy beam, polycrystal-izes it to this amorphous silicon thin film, and has a projection on a front face, and removing the projection of this polish recon thin film front face by chemical machinery polish using the polish slurry containing a polish abrasive grain. It is ****** by forming the source and a drain field in said barrier layer, after carrying out patterning of such a polish recon thin film, forming a barrier layer and forming gate dielectric film and a gate electrode on it to manufacture the thin film transistor of the forward stagger mold which has the good property which controlled thru/or canceled the poor withstand voltage of said gate dielectric film resulting from the projection of said polish recon thin film front face.
[0018] Especially, in the CMP process of said polish recon thin film, a silica particle is contained as a polish abrasive grain, and when pH uses the polishing slurry of 10-11, in order that said silica particle may react with the projection of said polish recon thin film, exfoliation removal of said reactant is carried out by mechanical polish from a polish recon thin film. That is, the projection of said polish recon thin film is removed alternatively, and can prevent film decrease of the polish recon thin film itself.
[0019] Moreover, it sets at the CMP process of said polish recon thin film, and is a pressure (load to the scouring pad 2 of the polish recon thin film in drawing 1 mentioned above) 20-1000kg/cm2 By carrying out, it becomes possible to

prevent the crack initiation of said polish recon thin film, and film decrease of a polish recon thin film.
[0020]
[Example] Hereafter, the desirable example of this invention is explained to a detail with reference to a drawing.
(Example 1) Said SiO2 as shown in (a) of drawing 2 , after forming SiO2 film 12 with a CVD method on a glass substrate 11 first The amorphous silicon (a-Si) thin film with a thickness of 0.05 micrometers was formed with the CVD method on the film 12. It continued and the laser beam with an energy density 250 - a 400 mJ/cm [2], and a pulse width of 20-30nm was irradiated at this a-Si thin film. Consequently, while said a-Si thin film was polycrystal-ized and was changed into the polish recon thin film 13, the projection 14 was generated on the front face.
[0021] Subsequently, make reverse the substrate 11 shown in the substrate holder 5 of the polishing equipment shown in drawing 1 mentioned above at (a) of drawing 2 , and it is held. the support shaft 4 of said holder 5 -- said substrate -- trade name [on a turntable 1] made from Rodale Press; -- Suba the scouring pad 2 which consists of 400 -- 100 g/cm2 A load is given. Making an opposite direction rotate said turntable 1 and holder 5 mutually at the rate of 60rpm, respectively By performing CMP actuation which supplies the polish slurry (the trade name made from FUJIMI; SP-15, pH=11) containing colloidal silica to said scouring pad 2 the rate for 20mL(s)/from a supply pipe 3 for 20 seconds, and removing the projection of the polish recon thin film 13 of said substrate 11 As shown in (b) of drawing 2 , flattening of the front face of the polish recon thin film 13 was carried out.
[0022] The optical surface roughness meter (Zygo) investigated five surface roughness and P-V (height between the maximum heights and the minimum crevice) in the polish recon thin film before and behind said CMP processing. Moreover, those five-point averages were calculated. The result is shown in the following table 1.
[0023]
[Table 1]

	研磨前		研磨後	
	表面粗さ (nm)	P－V (nm)	表面粗さ (nm)	P－V (nm)
No. 1	3.921	23.666	1.094	7.056
No. 2	2.503	18.744	1.107	7.087
No. 3	2.705	15.819	1.014	5.523
No. 4	2.364	15.299	1.099	6.363
No. 5	2.376	16.183	1.315	8.395
平均	2.774	17.942	1.126	6.885

[0024] It turns out that the five-point average P-V is set to about 7nm after polish to five-point average P-V of polycrystal-ized Ushiro's polish recon thin film having been 18nm so that clearly from said table 1, and flattening of the polish recon thin film front face is carried out.
[0025] Subsequently, as shown in (c) of drawing 3 , patterning of said polish recon thin film 13 was carried out according to the photo etching process, and the barrier layer 15 was formed. It is SiO2 with a thickness of 0.15 micrometers by the CVD method to the whole surface which continues and contains said barrier layer 15. After forming the film (gate dielectric film) 16, the gate electrode 17 was formed by depositing and carrying out patterning of the MoW film with a thickness of 0.25 micrometers. The source of n mold which pulls, continues, carries out the ion implantation of Lynn to said barrier layer 15 by using said gate electrode 17 as a mask, and is shown in (d) of drawing 3 by being activated, and the drain fields 18 and 19 were formed.
[0026] Subsequently, it is SiO2 by the CVD method to the whole surface. The interlayer insulation film 20 which consists of film was deposited. Then, opening of the contact holes 21 and 22 was carried out to said interlayer insulation film 20 part corresponding to said source and the drain fields 18 and 19, and the thin film transistor of the forward stagger mold shown in (e) of drawing 3 by performing deposition of aluminum film and patterning by forming said source, the source connected to the drain fields 18 and 19 through said contact holes 21 and 22, and the drain electrodes 23 and 24 was manufactured.
[0027] (Example 1 of a comparison) The thin film transistor of a forward stagger mold was manufactured by the same approach as an example 1 except having formed in the front face which does not perform CMP processing as a barrier layer with the polish recon thin film which the projection generated.
[0028] When the withstand voltage of the gate dielectric film of the thin film transistor of the acquired example 1 and

the example 1 of a comparison was measured, it was checked that the thin film transistor of an example 1 shows very high withstand voltage compared with the thin film transistor of the example 1 of a comparison.

[0029]

[Effect of the Invention] As explained above, according to this invention, by carrying out flattening of the high polish recon thin film front face of the mobility of a carrier, the gate dielectric film which has good withstand voltage can be formed on the barrier layer which consists of this polish recon thin film, as a result the manufacture approach of the thin film transistor of a reliable forward stagger mold can be offered.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of the thin film transistor of a forward stagger mold of having improved especially the barrier layer, about the manufacture approach of the thin film transistor included in a liquid crystal display.

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PRIOR ART

[Description of the Prior Art] The forward stagger mold thin film transistor included in a liquid crystal display formed the barrier layer in which the source and a drain field are formed conventionally with the amorphous silicon (a-Si is called hereafter) thin film. However, the a-Si thin film had the problem that the mobility of the carrier which has big effect on transistor characteristics was small.

[0003] Since it is such, in order to raise the property (mobility of a carrier) of the thin film transistor of a liquid crystal display in recent years, development of the technique which forms a barrier layer with a polish recon thin film is progressing. As a formation technique of this polish recon thin film, after forming an a-Si thin film to the insulator layer on a glass substrate, the approach of polycrystal-izing is learned by irradiating a energy beam like a laser beam.

[0004] However, a dozens of nm projection generates the polish recon thin film obtained by said approach on a front face. For this reason, if the source and a drain field are formed in said barrier layer and the thin film transistor of a forward stagger mold is manufactured after carrying out patterning of this polish recon thin film, forming a barrier layer and forming gate dielectric film and a gate electrode on it, it will originate in the projection on the front face of a barrier layer which consists of said polish recon, the poor proof pressure of said gate dielectric film will be produced, and transistor characteristics will fall remarkably.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, by carrying out flattening of the high polish recon thin film front face of the mobility of a carrier, the gate dielectric film which has good withstand voltage can be formed on the barrier layer which consists of this polish recon thin film, as a result the manufacture approach of the thin film transistor of a reliable forward stagger mold can be offered.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The purpose of this invention tends to offer the manufacture approach of the thin film transistor of the forward stagger mold which can form the gate dielectric film which has good withstand voltage on the barrier layer which consists of this polish recon thin film by carrying out flattening of the high polish recon thin film front face of the mobility of a carrier.

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MEANS

[Means for Solving the Problem] The manufacture approach of the thin film transistor concerning this invention is characterized by to provide the process which forms an amorphous silicon thin film to the insulator layer on a glass substrate, the process which irradiates a energy beam, polycrystal-izes it to said amorphous silicon thin film, and forms a polish recon thin film, and the process which removes the projection of said polish recon thin film front face by chemical-machinery polish using the polish slurry containing a polish abrasive grain, and carries out flattening of said polish recon thin film front face.
[0007]
[Embodiment of the Invention] Hereafter, the manufacture approach of the thin film transistor concerning this invention is explained to a detail.
(The 1st process) An a-Si thin film is first formed with a CVD method etc. to an insulator layer like the silicon oxide on a glass substrate.
[0008] It permits forming a gate electrode beforehand before covering of said insulator layer on said glass substrate.
(The 2nd process) Subsequently to said a-Si thin film, a energy beam is irradiated. At this time, said a-Si thin film is polycrystal-ized, and is changed into a polish recon thin film with good crystallinity. The projection of dozens of nm order occurs on a front face in coincidence.
[0009] As said energy beam, a laser beam, an electron beam, etc. can be used, for example.
(The 3rd process) By [which subsequently used the polish slurry which includes said polish recon thin film front face for a polish abrasive grain] carrying out chemical machinery polish (CMP;Chemical Mechanical Polishing), said projection is removed and flattening of the front face of said polish RINKO thin film is carried out.
[0010] As polishing equipment applied to said CMP, the thing of the structure shown, for example in drawing 1 is used. This polishing equipment has a turntable 1. On this turntable 1, the scouring pad 2 made from cloth is covered. The supply pipe 3 for supplying polish liquid is arranged above said scouring pad 2. The substrate holder 5 which has the support shaft 4 on the top face is arranged can move up and down freely above a scouring pad 2, and free [rotation].
[0011] Supplying the polishing liquid 7 of the presentation which held in such polishing equipment so that the polish recon thin film which is the polished surface might counter said scouring pad 2 in a substrate 6 with said holder 5, and was mentioned above from said supply pipe 3 Said substrate 6 is turned to said scouring pad 2 with said support shaft 4, a desired load is given, and the projection of the polish recon thin film front face on said substrate 6 is removed by making an opposite direction rotate said HORUDO 5 and said turntable 1 of each other further.
[0012] As said polish abrasive grain, the particle of at least one ingredient chosen from a silica, a zirconia, cerium oxide, and an alumina can be used. These particles have the mean particle diameter of 0.02-0.1 micrometers, and it is desirable spherical or to have the configuration approximated to the ball.
[0013] As for said polish abrasive grain, it is desirable to contain 0.1 to 30% of the weight in said polish slurry. If the content of said polish abrasive grain is carried out to less than 0.1% of the weight, it will become difficult to fully attain the effectiveness. On the other hand, if the content of said polish abrasive grain exceeds 30 % of the weight, the viscosity of polish liquid etc. will become high and it will be hard coming to deal with it. The content of said more desirable polish abrasive grain is 1 - 10 % of the weight.
[0014] Said especially polish abrasive grain has a desirable silica particle (preferably colloidal silica with a mean particle diameter of 0.01-0.09 micrometers). When the polish abrasive grain which consists of such a silica particle is used, it is desirable to set pH of said polish slurry to 10-11.
[0015] The pressure (load to the scouring pad 2 of the polish recon thin film in drawing 1 mentioned above) in said CMP is 20-1000kg/cm2. Carrying out is desirable. It is said pressure 20kg/cm2 If it is made the following, it will become difficult to remove the projection of said polish recon thin film. On the other hand, said pressure is

1000kg/cm2. When it exceeds, a crack occurs in a polish recon thin film, or a possibility that the thickness of a polish recon thin film decreases and of producing the so-called film decrease is in it. said more desirable pressure -- 50-200kg/cm2 it is .

[0016] (The 4th process) said barrier layer after the front face mentioned above carries out patterning of the flat polish recon thin film according to a photo etching process and forms a barrier layer -- gate dielectric film is formed in a top face at least. After continuing and forming a gate electrode on the gate dielectric film corresponding to said barrier layer, the ion implantation of the impurity which gives conductivity to said barrier layer by using said gate electrode as a mask is carried out, and the source and a drain field are formed. It pulls, and it continues and an interlayer insulation film is deposited on the whole surface with a CVD method. then, said interlayer insulation film part corresponding to said source and a drain field -- a contact hole -- opening -- carrying out -- an electrode -- public funds -- the thin film transistor of a forward stagger mold is manufactured by forming the source and the drain electrode which are connected to said source and a drain field through said contact hole by covering of a group, and patterning.

[0017] A front face can make it the polish recon thin film by which flattening was carried out by according to this invention explained above, forming an amorphous silicon thin film to the insulator layer on a glass substrate, forming the polish recon thin film which irradiates a energy beam, polycrystal-izes it to this amorphous silicon thin film, and has a projection on a front face, and removing the projection of this polish recon thin film front face by chemical machinery polish using the polish slurry containing a polish abrasive grain. It is ****** by forming the source and a drain field in said barrier layer, after carrying out patterning of such a polish recon thin film, forming a barrier layer and forming gate dielectric film and a gate electrode on it to manufacture the thin film transistor of the forward stagger mold which has the good property which controlled thru/or canceled the poor withstand voltage of said gate dielectric film resulting from the projection of said polish recon thin film front face.

[0018] Especially, in the CMP process of said polish recon thin film, a silica particle is contained as a polish abrasive grain, and when pH uses the polishing slurry of 10-11, in order that said silica particle may react with the projection of said polish recon thin film, exfoliation removal of said reactant is carried out by mechanical polish from a polish recon thin film. That is, the projection of said polish recon thin film is removed alternatively, and can prevent film decrease of the polish recon thin film itself.

[0019] Moreover, it sets at the CMP process of said polish recon thin film, and is a pressure (load to the scouring pad 2 of the polish recon thin film in drawing 1 mentioned above) 20-1000kg/cm2 By carrying out, it becomes possible to prevent the crack initiation of said polish recon thin film, and film decrease of a polish recon thin film.

[Translation done.]

* NOTICES *

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EXAMPLE

[Example] Hereafter, the desirable example of this invention is explained to a detail with reference to a drawing. (Example 1) Said SiO2 as shown in (a) of drawing 2 , after forming SiO2 film 12 with a CVD method on a glass substrate 11 first The amorphous silicon (a-Si) thin film with a thickness of 0.05 micrometers was formed with the CVD method on the film 12. It continued and the laser beam with an energy density 250 - a 400 mJ/cm [2], and a pulse width of 20-30nm was irradiated at this a-Si thin film. Consequently, while said a-Si thin film was polycrystal-ized and was changed into the polish recon thin film 13, the projection 14 was generated on the front face.
[0021] Subsequently, make reverse the substrate 11 shown in the substrate holder 5 of the polishing equipment shown in drawing 1 mentioned above at (a) of drawing 2 , and it is held. the support shaft 4 of said holder 5 -- said substrate -- trade name [on a turntable 1] made from Rodale Press; -- Suba the scouring pad 2 which consists of 400 -- 100 g/cm2 A load is given. Making an opposite direction rotate said turntable 1 and holder 5 mutually at the rate of 60rpm, respectively By performing CMP actuation which supplies the polish slurry (the trade name made from FUJIMI; SP-15, pH=11) containing colloidal silica to said scouring pad 2 the rate for 20mL(s)/from a supply pipe 3 for 20 seconds, and removing the projection of the polish recon thin film 13 of said substrate 11 As shown in (b) of drawing 2 , flattening of the front face of the polish recon thin film 13 was carried out.
[0022] The optical surface roughness meter (Zygo) investigated five surface roughness and P-V (height between the maximum heights and the minimum crevice) in the polish recon thin film before and behind said CMP processing. Moreover, those five-point averages were calculated. The result is shown in the following table 1.
[0023]
[Table 1]

	研磨前		研磨後	
	表面粗さ (nm)	P－V (nm)	表面粗さ (nm)	P－V (nm)
No. 1	3.921	23.666	1.094	7.056
No. 2	2.503	18.744	1.107	7.087
No. 3	2.705	15.819	1.014	5.523
No. 4	2.364	15.299	1.099	6.383
No. 5	2.376	16.183	1.315	8.395
平均	2.774	17.942	1.126	6.885

[0024] It turns out that the five-point average P-V is set to about 7nm after polish to five-point average P-V of polycrystal-ized Ushiro's polish recon thin film having been 18nm so that clearly from said table 1, and flattening of the polish recon thin film front face is carried out.
[0025] Subsequently, as shown in (c) of drawing 3 , patterning of said polish recon thin film 13 was carried out according to the photo etching process, and the barrier layer 15 was formed. It is SiO2 with a thickness of 0.15 micrometers by the CVD method to the whole surface which continues and contains said barrier layer 15. After forming the film (gate dielectric film) 16, the gate electrode 17 was formed by depositing and carrying out patterning of the MoW film with a thickness of 0.25 micrometers. The source of n mold which pulls, continues, carries out the ion implantation of Lynn to said barrier layer 15 by using said gate electrode 17 as a mask, and is shown in (d) of drawing 3 by being activated, and the drain fields 18 and 19 were formed.
[0026] Subsequently, it is SiO2 by the CVD method to the whole surface. The interlayer insulation film 20 which

consists of film was deposited. Then, opening of the contact holes 21 and 22 was carried out to said interlayer insulation film 20 part corresponding to said source and the drain fields 18 and 19, and the thin film transistor of the forward stagger mold shown in (e) of drawing 3 by performing deposition of aluminum film and patterning by forming said source, the source connected to the drain fields 18 and 19 through said contact holes 21 and 22, and the drain electrodes 23 and 24 was manufactured.

[0027] (Example 1 of a comparison) The thin film transistor of a forward stagger mold was manufactured by the same approach as an example 1 except having formed in the front face which does not perform CMP processing as a barrier layer with the polish recon thin film which the projection generated.

[0028] When the withstand voltage of the gate dielectric film of the thin film transistor of the acquired example 1 and the example 1 of a comparison was measured, it was checked that the thin film transistor of an example 1 shows very high withstand voltage compared with the thin film transistor of the example 1 of a comparison.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The schematic diagram showing the polishing equipment used for the CMP process of this invention.
[Drawing 2] The sectional view showing the production process of the forward stagger mold thin film transistor in the example 1 of this invention.
[Drawing 3] The sectional view showing the production process of the forward stagger mold thin film transistor in the example 1 of this invention.
[Description of Notations]
1 -- Turntable,
2 -- Scouring pad
3 -- Supply pipe,
5 -- Holder,
11 -- Glass substrate
13 -- Polish recon thin film,
14 -- Projection,
15 -- Barrier layer,
16 -- Gate dielectric film
17 -- Gate electrode.

[Translation done.]

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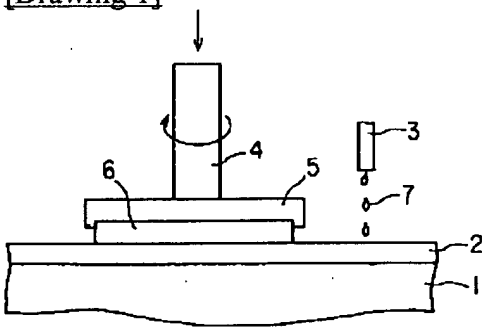
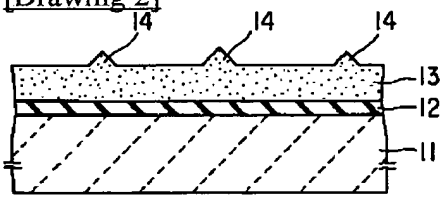
DRAWINGS

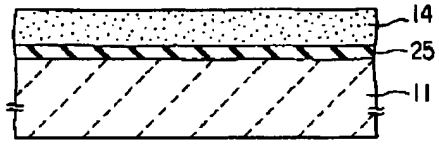
[Drawing 1]



[Drawing 2]

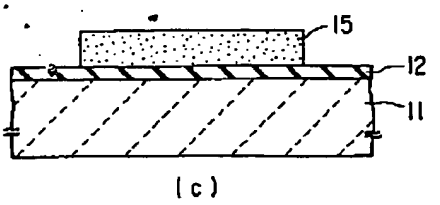


(a)

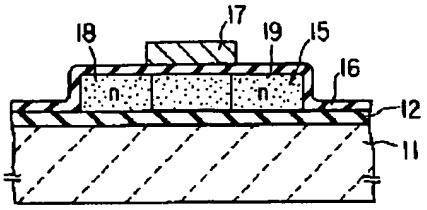


(b)

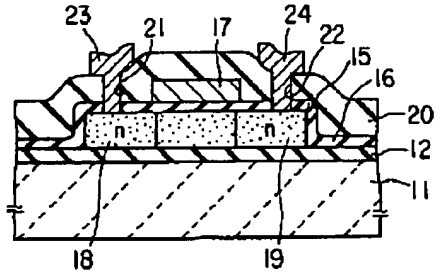
[Drawing 3]



(c)



(d)



(e)

[Translation done.]